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Fig. 1a

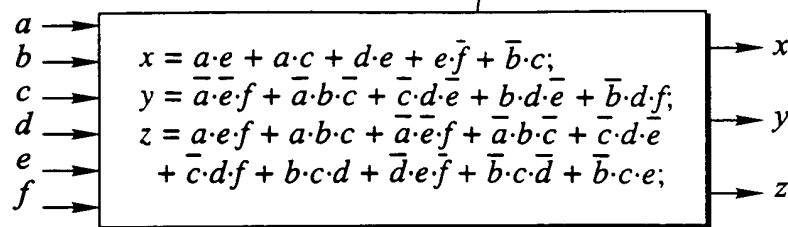


Fig. 1b

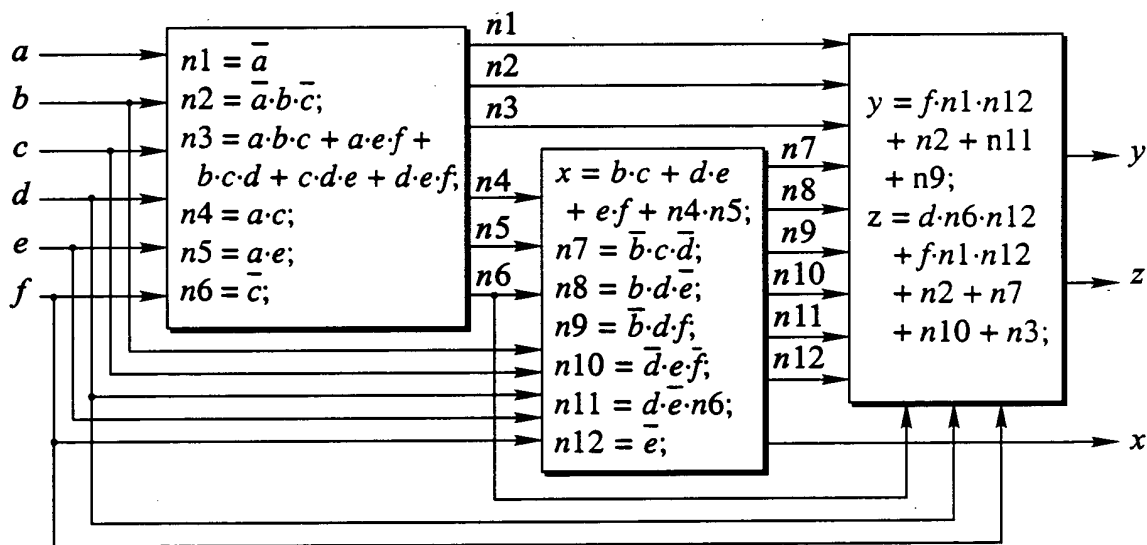
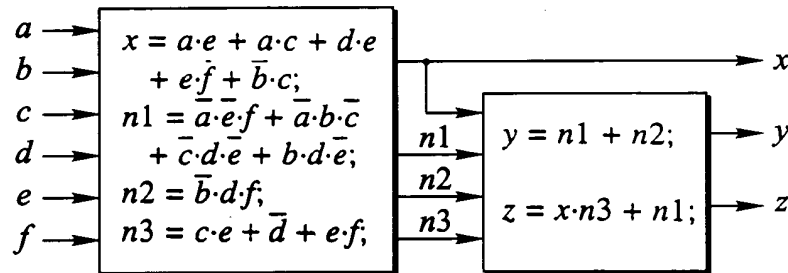
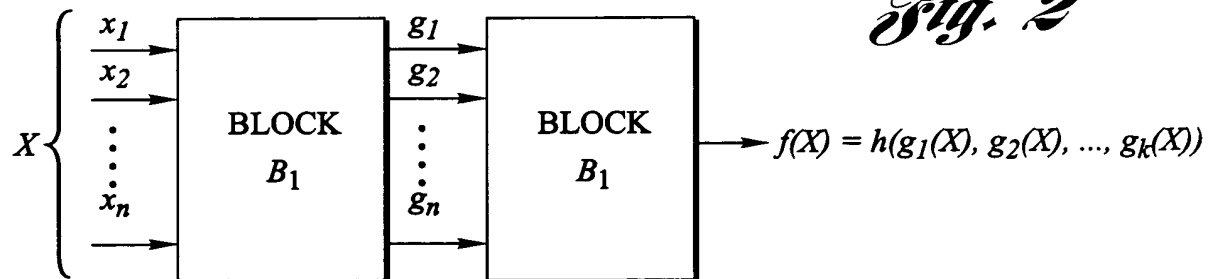


Fig. 1c

Fig. 2



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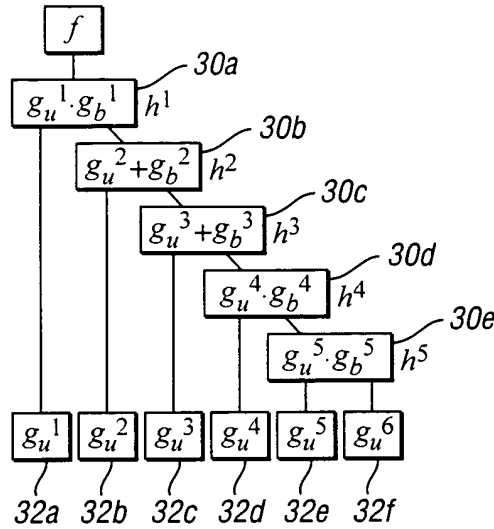


Fig. 3a

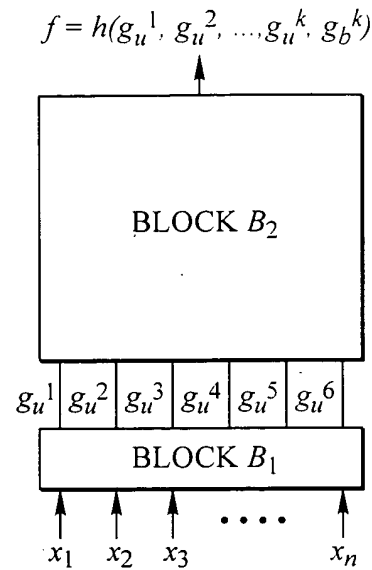


Fig. 3b

Fig. 4

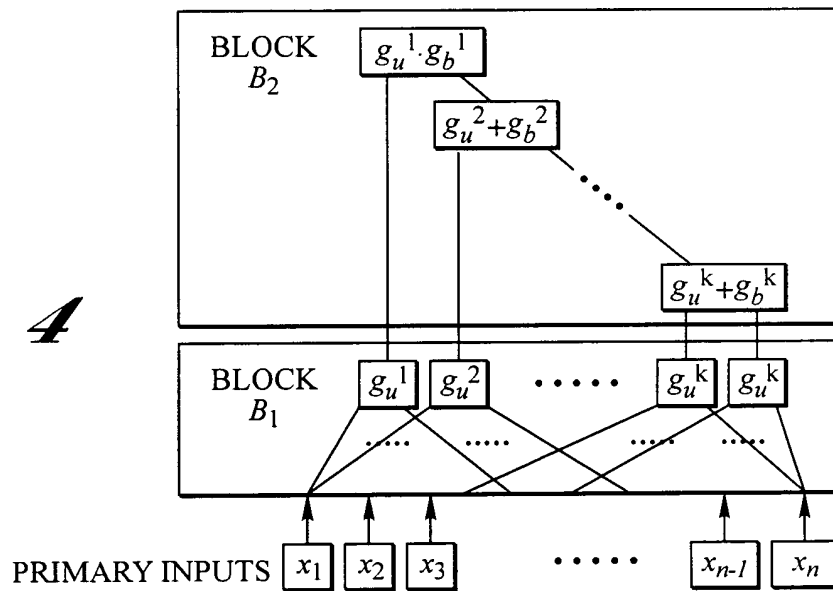
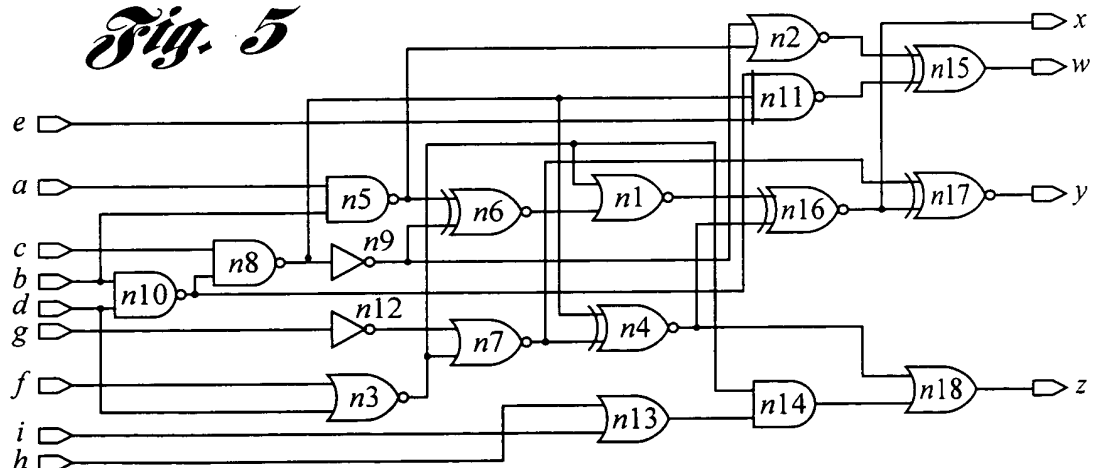


Fig. 5



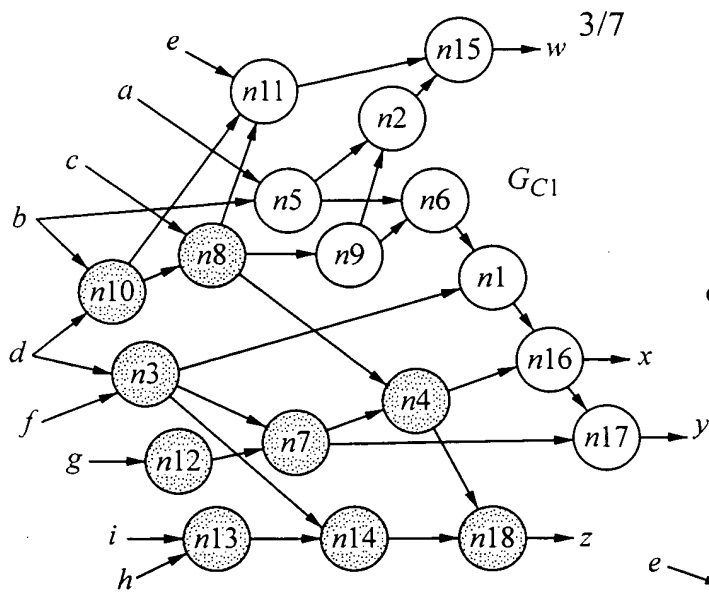


Fig. 6a

Fig. 6b

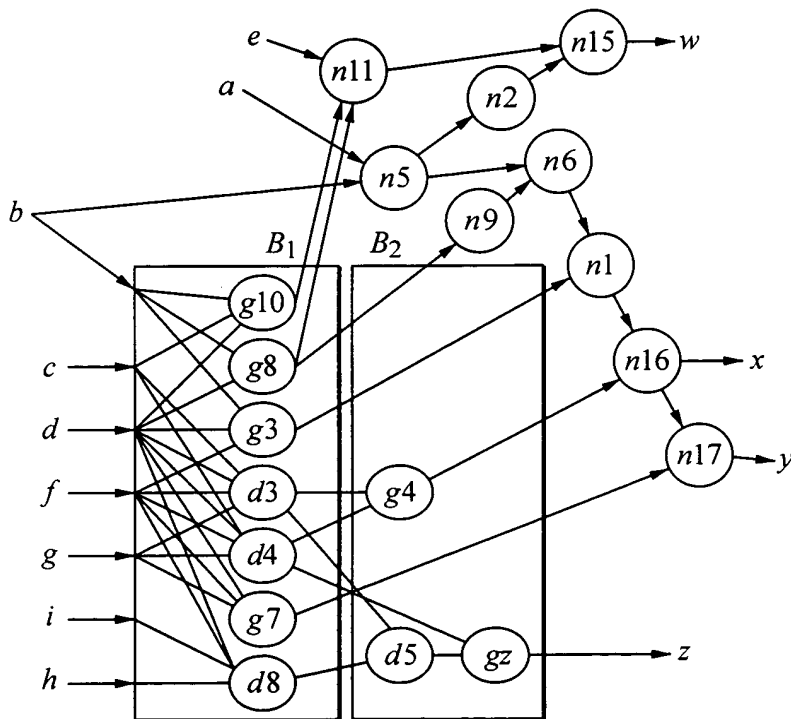
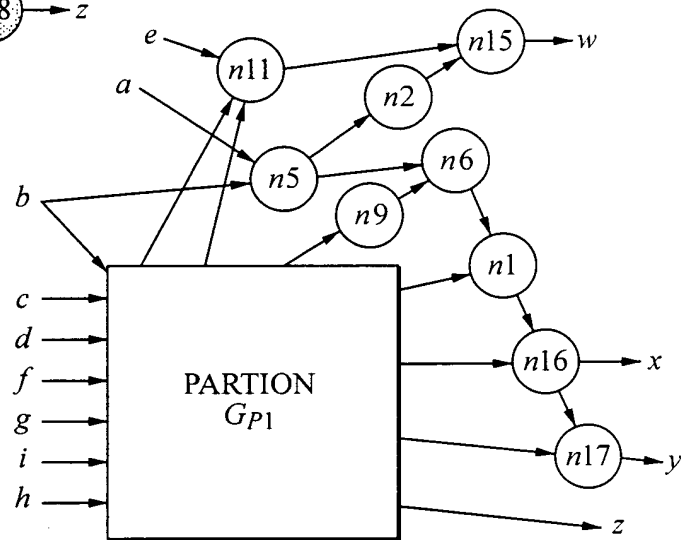


Fig. 6c

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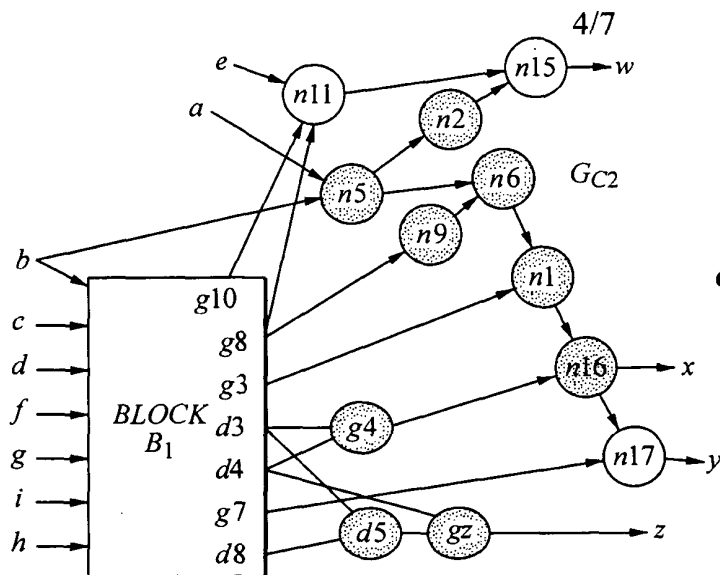


Fig. 6d

Fig. 6e

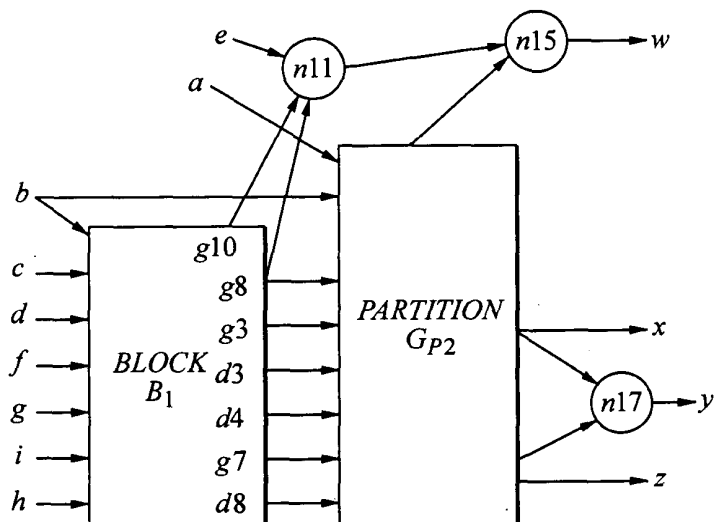
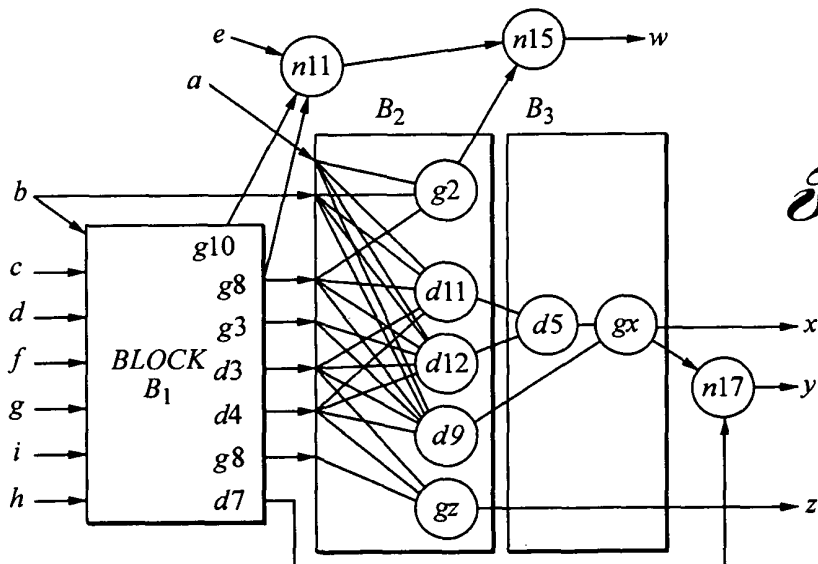


Fig. 6f



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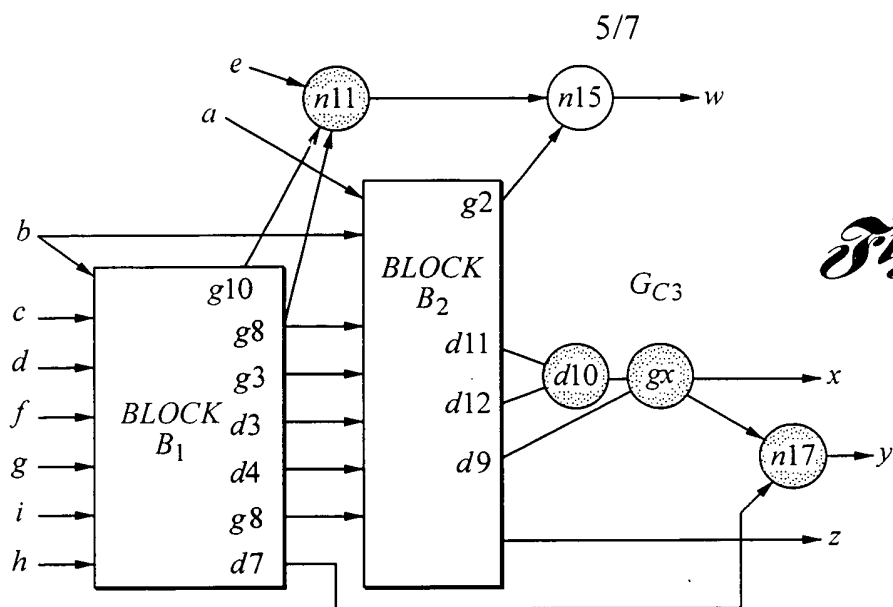


Fig. 6h

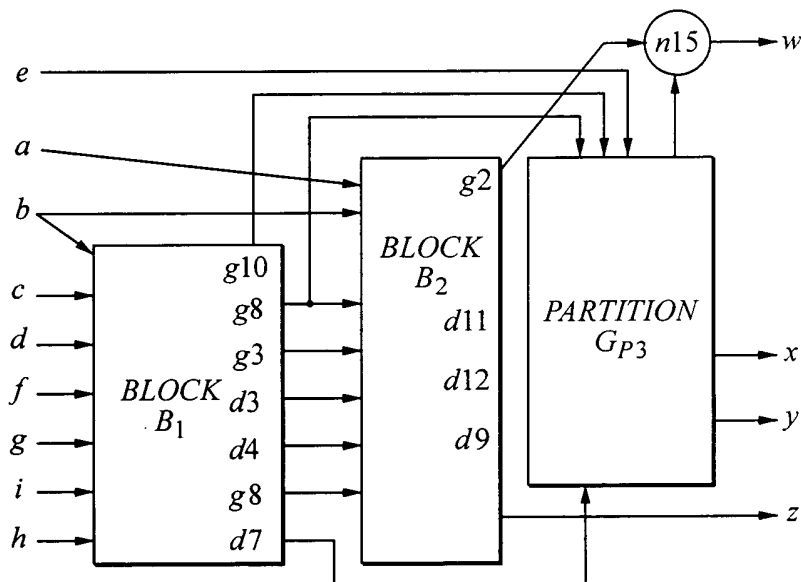
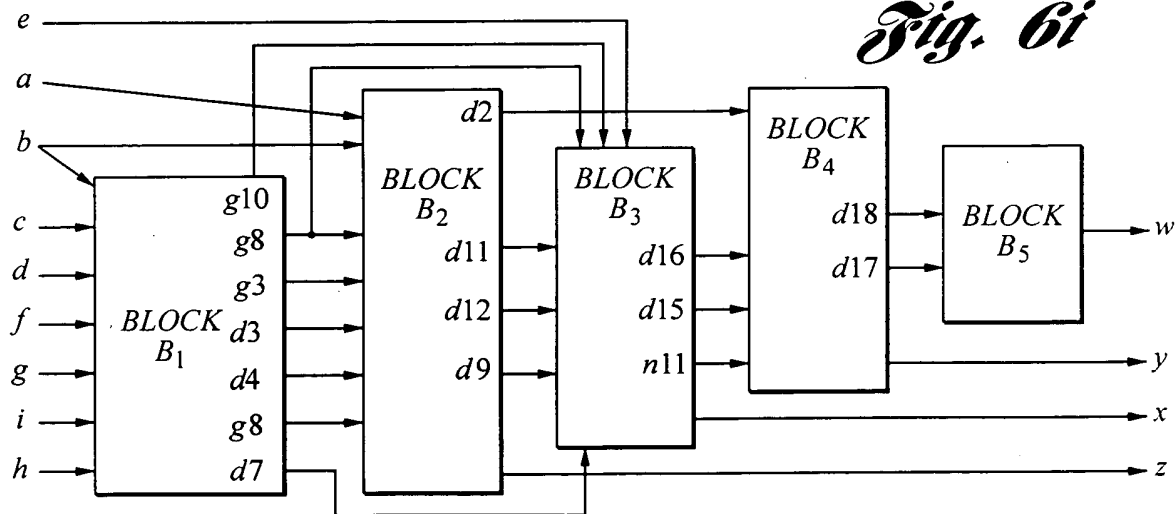


Fig. 6i



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The diagram shows a logic network with three internal nodes: a , b , and c . Node a is at the top, connected to nodes c and b . Node c is connected to node b . Node b is connected to two output nodes, 0 and 1 . Node a is also connected to output node 1 . The diagram includes labels f_4^{SOP} and $\bar{c}\bar{b}$.

```

graph TD
    a((a)) -- 0 --> b1((b))
    a -- 1 --> c1((c))
    b1 -- 1 --> c2((c))
    b1 -- 0 --> 0_1[0]
    c1 -- 1 --> b2((b))
    c1 -- 0 --> 0_2[0]
    c2 -- 0 --> 0_1
    c2 -- 1 --> 1_1[1]
    b2 -- 0 --> 1_1
    b2 -- 1 --> 0_2
    style 0_1 fill:#fff,stroke:#000,stroke-width:1px
    style 1_1 fill:#fff,stroke:#000,stroke-width:1px

```

Fig. 8a

